CLAIM AMENDMENTS

Claim Amendment Summary

Claims pending

- Before this Amendment: Claims 1–10, and 25-35
- After this Amendment: Claims 1–10, 25-30 and 32-35

Non-Elected, Canceled, or Withdrawn claims: 31

Amended claims: 25, 34, and 35

New claims: None

Claims:

1. (Previously Presented) A fractional-type phase-locked loop circuit for synthesizing an output signal by multiplying a frequency of a reference signal by a fractional conversion factor, the circuit including: means for generating a modulation value, means for generating a feedback signal by dividing the frequency of the output signal by a dividing ratio, the dividing ratio being modulated according to the modulation value for providing the conversion factor on an average, means for generating a control signal indicative of a phase difference between the reference signal and the feedback signal, means for controlling the frequency of the output signal according to the control signal, and means for compensating a phase error caused by the modulation of the dividing ratio, wherein

the means for compensating includes means for calculating an incremental value, indicative of an incremental phase error, according to the conversion factor and the modulation value, means for calculating a correction value accumulating the incremental value, and means for conditioning the control signal according to the correction value.

2. (Original) The circuit according to claim 1, wherein the means for generating the modulation value includes a sigma-delta modulator having an order at least equal to two.

3. (Original) The circuit according to claim 1, wherein the means for generating the modulation value includes a multi-bit modulator.

4. (Original) The circuit according to claim 1, wherein the means for generating the modulation value is responsive to an adjusting value consisting of an integer varying from zero to a pre-defined modulus, the means for calculating the incremental value including means for calculating a first value multiplying the modulation value by the pre-defined modulus and means for calculating a second value subtracting the first value from the adjusting value, and wherein the means for calculating the correction value includes means for accumulating the second value and means for scaling the accumulated second value according to the pre-defined modulus and the conversion factor.

5. (Original) The circuit according to claim 1, wherein the means for conditioning includes means for converting a representation of the correction value into a thermometric code consisting of a plurality of thermometric digits of even weight, and a plurality of digital-to-analog converters each one for a corresponding thermometric digit.

6. (Original) The circuit according to claim 5, wherein each thermometric digit consists of a thermometric bit, each digital-to-analog converter being a single-bit converter.

7. (Original) The circuit according to claim 6, wherein the correction value consists of a signed value, the digital-to-analog converters consisting of a first plurality of the single-bit converters each one for a corresponding thermometric bit representing a module of the correction value when positive and a second plurality of single-bit converters each one for a corresponding thermometric bit representing the module of the correction value when negative.

8. (Original) The circuit according to claim 5, wherein the means for conditioning further includes means for scrambling the thermometric digits.

9. (Original) The circuit according to claim 8, wherein the means for scrambling includes means for re-arranging the thermometric digits according to a random algorithm or a barrel shift algorithm.

10. (Previously Presented) In a fractional-type phase-locked loop circuit, a method of synthesizing an output signal multiplying a frequency of a reference signal by a fractional conversion factor, the method including the steps of:

generating a modulation value with a modulator,

generating a feedback signal dividing the frequency of the output signal by a dividing ratio, the dividing ratio being modulated according to the modulation value for providing the conversion factor on the average,

generating a control signal indicative of a phase difference between the reference signal and the feedback signal,

controlling the frequency of the output signal according to the control signal, and

compensating a phase error caused by the modulation of the dividing ratio, wherein the step of compensating includes:

calculating an incremental value, indicative of an incremental phase error, according to the conversion factor and the modulation value,

calculating a correction value accumulating the incremental value, and

conditioning the control signal according to the correction value.

11-24. (Canceled)

25. (Currently Amended) A phase-locked loop, comprising:

a phase-frequency detector operable to generate a phase-error signal based on a comparison of a reference signal and a feedback signal;

a control circuit coupled to the phase-frequency detector and operable to generate a digital conditioning signal based on a modulation value and the feedback signal; and

a generator coupled to the control circuit and the phase-frequency detector and operable to receive a control signal to generate an output signal, the control signal based on a summation of the phase-error signal and an analog conversion of the digital conditioning signal;

wherein the feedback signal comprises a signal having a frequency of the output signal divided by a dividing ratio, the dividing ratio being modulated according to the modulation value.

26. (Previously Presented) A phase-locked loop, comprising:

a phase-frequency detector operable to generate a phase-error signal based on a comparison of a reference signal and a feedback signal;

a control circuit coupled to the phase-frequency detector and operable to generate a conditioning signal based on a modulation value and the feedback signal; and

a generator coupled to the control circuit and the phase-frequency detector and operable to receive a control signal to generate an output signal, the control signal based on a summation of the phase-error signal and conditioning signal, wherein the control circuit comprises:

a sigma-delta modulator operable to generate the modulation value

a control logic block coupled to the sigma-delta modulator and operable to generate a correction value based on the modulation value and an adjusting value, the control logic block clocked by the feedback signal; and

a digital-to-analog converter coupled to the control logic block operable to generate the conditioning signal based on the correction value.

27. (Previously Presented) A phase-locked loop, comprising:

a phase-frequency detector operable to generate a phase-error signal based on a comparison of a reference signal and a feedback signal;

a control circuit coupled to the phase-frequency detector and operable to generate a conditioning signal based on a modulation value and the feedback signal; and

a generator coupled to the control circuit and the phase-frequency detector and operable to receive a control signal to generate an output signal, the control signal based on a summation of the phase-error signal and conditioning signal;

wherein the control circuit comprises:

a sigma-delta modulator operable to generate the modulation value;

a control logic block coupled to the sigma-delta modulator and operable to generate a correction value based on the modulation value and an adjusting value, the control logic block clocked by the feedback signal;

a digital-to-analog converter coupled to the control logic block operable to generate the conditioning signal based on the correction value; and

wherein the sigma-delta generator comprises a first modifier operable to convert a first data set corresponding to the adjusting value into a second data set.

28. (Previously presented) The phase-locked loop of claim 27 wherein the sigma-delta generator further comprises a second modifier coupled to the first modifier, the second modifier operable to convert the second data set into the modulation value.

29. (Previously presented) The phase-locked loop of claim 25, further comprising a filter coupled to the generator and operable to filter the control signal before the control signal is received by the generator.

30. (Previously presented) The phase-locked loop of claim 25, further comprising a multi-modulus frequency divider coupled to the phase-frequency detector and operable to modify the feedback signal based on the modulation value.

31. (Canceled)

32. (Previously Presented) A method for controlling the output of a phase-locked loop, the method comprising:

determining a phase difference between a reference signal and a feedback signal with a phase frequency detector;

generating a phase-error signal from the determined phase difference;

generating a conditioning signal based upon a modulation value and the feedback signal;

modifying the phase-error signal with the conditioning signal; and

generating an output signal with a generator from the modified phase-error signal;

wherein generating the conditioning signal comprises:

generating a first data set based on an adjusting value

generating a second data set based on a the first set of data and modulation value; and

generating the conditioning signal based on the second data set.

33. (Previously presented) The method of claim 32, further comprising generating the feedback signal based on the output signal and the modulation value.

34. (Currently Amended) The method of claim [[31]] 32, further comprising filtering the modified phase-error signal.

35. (Currently Amended) An electronic system, comprising:

a phase-locked loop, comprising:

a phase-frequency detector operable to generate a phase-error signal based on a comparison of a reference signal and a feedback signal;

a control circuit coupled to the phase-frequency detector and operable to generate a digital conditioning signal based on a modulation value and the feedback signal; and

a generator coupled to the control circuit and the phase-frequency detector and operable to receive a control signal to generate an output signal, the control signal based on a summation of the phase-error signal and analog conversion of the digital conditioning signal;

wherein the feedback signal comprises a signal having a frequency of the output signal divided by a dividing ratio, the dividing ratio being modulated according to the modulation value.